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Attorney's Docket No.: 42P15677

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:)
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Scott A. Hareland et al.) Examiner: Pham, Hoai V.
)
Application No.: 10/607,632) Art Unit: 2814
)
Filed: June 27, 2003)
)
For: NONPLANAR DEVICE WITH STRESS)
INCORPORATION LAYER AND METHODS)
OF FABRICATION)

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

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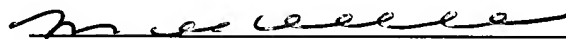
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Respectfully submitted,

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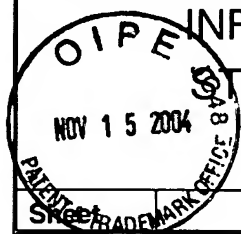
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INFORMATION DISCLOSURE

STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known

Application Number	10/607,632
Filing Date	June 27, 2003
First Named Inventor:	Scott A. Hareland
Art Unit	2814
Examiner Name	Pham, Hoai V.
Attorney Docket Number	42P15677

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)				
		US-	6,483,156 B1	11/19/2002	Adkission et al.	
		US-	6,413,802 B1	7/2/2002	Hu et al.	
		US-	5,578,513	11/26/1996	Maegawa	
		US-				
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FOREIGN PATENT DOCUMENTS

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		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
		EP	0 623 963 A1		11/9/1994	Siemens AG		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <small>(use as many sheets as necessary)</small>				Application Number	10/607,632
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				Art Unit	2814
				Examiner Name	Pham. Hoai V.
				Attorney Docket Number	42P15677
Sheet	2	of	2		
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
		International Search Report PCT/US03/26242			
		International Search Report PCT/US 03/40320			
		V. Subramanian et al., "A Bulk-Si-Compatible Ultrathin-body SOI Technology for Sub-100m MOSFETS" Proceeding of the 57th Annual Device Research Conference, pp. 28-29 (1999)			
		Hisamoto et al., "A Folded-channel MOSFET for Deepsub-tenth Micron Era", 1998 IEEE International Electron Device Meeting Technical Digest, pp 1032-1034 (1998)			
		Huang et al., "Sub 50-nm FinFET: PMOS", 1999 IEEE International Electron Device Meeting Technical Digest, pp 67-70 (1999)			
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		Hisamoto et al., "A Fully Depleted Lean-Channel Transistor (DELTA)-A Novel Vertical Ultrathin SOI MOSFET", IEEE Electron Device Letters, V. 11(1), pp36-38 (1990).			
		Jong-Tae Park et al., "Pi-Gate SOI MOSFET" IEEE Electron Device Letters, Vol. 22, No. 8, August 2001, pages 405-406			
		Hisamoto, Digh et al. "FinFET- A Self-Aligned Double-Gate MOSFET Scalable to 20 nm", IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325			

Examiner Signature	Date Considered	
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